CLAIMS

What is claimed is:

1. A method of processing samples comprising:

reading the samples into a tapped delay chain;

processing samples from taps on the delay chain;

subsequent to a processing event, shifting samples rapidly from the delay chain at a higher rate than samples coming in; and

reducing the length of the delay chain.

2. The method of Claim 1 wherein the samples are from a data packet.

3. The method of Claim 2 wherein the data packet conforms to 802.11 standards.

4. The method of Claim 3 wherein the event includes a synchronization of the data packet.

5. The method of Claim 4 wherein the delay chain comprises a plurality of pipelined registers

6. The method of Claim 5 wherein the method is repeated to further reduce the length of the delay chain.

7. The method of Claim 5 wherein reducing the length of the delay chain is performed by bypassing empty registers;.

8. A method of processing samples of a data packet comprising:

reading the samples from a data packet into a tapped delay chain comprising a plurality of pipelined registers;

processing samples from taps on the delay chain to synchronize a data packet;

subsequent to synchronization of the data packet, shifting samples rapidly from the delay chain at a higher rate than samples coming in;

reducing the length of the delay chain by bypassing empty registers; and

repeating the steps of shifting samples rapidly and reducing the length of the delay chain.

9. An apparatus comprising:

a pipeline of registers that store data samples;

logic circuitry which controls the output of each individual register from the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor which controls the data shifting rates, the logic circuitry, and the output of the multiplexer.

10. An apparatus of Claim 9 wherein the data samples are from a data packet.

11. An apparatus of Claim 10 data packet conforms to 802.11 standards.

12. An apparatus of Claim 11 further comprising a timing recovery module for synchronization of the data packet that initiates a transition in the processor.

13. An apparatus comprising:

a pipeline of registers that stores data samples of a data packet;

a timing recovery module for synchronization of the data packet that initiates a transition;

a logic circuitry which controls the output of each individual register from the pipeline of registers;

a multiplexer having inputs from select registers from the pipeline of registers, and an output; and

a processor having inputs from a timing recovery module for packet synchronization which controls the data shifting rates, the logic circuitry, and the output of the multiplexer.

14. An apparatus comprising:

means for reading data samples into a tapped delay chain;

means for processing data samples from taps on the delay chain;

means for shifting data samples rapidly from the delay chain at a higher rate than data samples coming in; and

means for reducing the length of the delay chain.